

## **AMENDMENTS TO THE CLAIMS**

- 1        130. An integrated circuit device comprising:
  - 2            a circuit to convert an input value into a search value;
  - 3            a first storage including content addressable memory (CAM) cells, compare lines
  - 4            coupled to columns of the CAM cells and match lines coupled to rows of the
  - 5            CAM cells, the compare lines being coupled to receive the search value;
  - 6            a second storage coupled to the match lines of the first storage; and
  - 7            a compare circuit coupled to an output of the second storage and coupled to receive
  - 8            the input value.
- 1        131. The integrated circuit device of claim 130 wherein the second storage comprises an array of static random access memory (SRAM) cells.
- 1        132. The integrated circuit device of claim 130 wherein the second storage comprises an array of dynamic random access memory (DRAM) cells.
- 1        133. The integrated circuit device of claim 130 wherein each of the CAM cells  
2            comprises a compare circuit coupled to at least one of the compare lines and at least  
3            one of the match lines.
- 1        134. The integrated circuit device of claim 130 wherein the CAM cells within a column  
2            of the CAM cells comprise respective compare circuits coupled to a common pair  
3            of compare lines and to respective match lines.
- 1        135. The integrated circuit device of claim 130 wherein the first storage further includes

2 word lines coupled to the rows of the CAM cells.

1 136. The integrated circuit device of claim 130 further comprising a select circuit having  
2 a first input port coupled to the word lines and a second input port coupled to the  
3 match lines.

1 137. The integrated circuit device of claim 136 wherein the second storage comprises  
2 word lines coupled to an output of the select circuit.

1 138. The integrated circuit device of claim 137 wherein the select circuit is responsive to  
2 an operation select signal to select either a decoded row address present on the word  
3 lines of the first storage or match signals present on the match lines of the first  
4 storage to be output onto the word lines of the second storage.

1 139. The integrated circuit device of claim 130 wherein the circuit to convert the input  
2 value into a search value is a cyclic redundancy check (CRC) circuit that generates  
3 a CRC value based on the input value, and wherein at least a portion of the CRC  
4 value constitutes the search value.

1 140. The integrated circuit device of claim 130 further comprising an interface and an  
2 assembler circuit coupled to the interface, the assembler circuit being configured to  
3 reorder selected bits within a value received via the interface to generate the input  
4 value.

1 141. The integrated circuit device of claim 130 wherein the circuit to convert the input  
2 value comprises a mask circuit to mask selected bits in the input value.

- 1        142. A content addressable memory (CAM) comprising:
  - 2              a cyclic redundancy check (CRC) circuit to generate a CRC value; and
  - 3              a CAM array having compare lines coupled to the CRC circuit to receive at least a
  - 4              portion of the CRC value therefrom.
- 1        143. The CAM of claim 142 wherein the CAM further comprises a mask circuit to mask selected bits in the CRC value.
- 1        144. The CAM of claim 143 further comprising a configuration circuit to store a configuration value indicative of the selected bits to be masked within the CRC value, the configuration circuit being coupled to the mask circuit to provide the configuration value thereto.
- 1        145. The CAM of claim 142 wherein the CRC value comprises N constituent bits and wherein the at least a portion of the CRC value comprises M contiguous bits of the CRC value, M being less than N.
- 1        146. A content addressable memory comprising:
  - 2              a CAM array including a plurality of CAM cells and a plurality of match lines coupled to respective rows of the CAM cells;
  - 4              a priority index table including a plurality of priority storage circuits coupled to store respective priority values and coupled respectively to the plurality of match lines; and
  - 7              a multiplexer having a first input coupled to receive a selected priority value from

8           the priority index table, and a second input to receive a predetermined priority  
9           value.

1       147. The CAM of claim 146 wherein the priority values indicate relative priorities of  
2           values stored within corresponding rows of the CAM cells.

1       148. The CAM of claim 146 wherein the multiplexer is responsive to a select signal to  
2           output either the selected priority value or the predetermined priority value.

1       149. The CAM of claim 146 wherein the multiplexer is configured to output the  
2           predetermined priority value in response to an operation to determine whether the  
3           CAM is able to store a first value, and wherein the multiplexer is configured to  
4           output the selected priority value in response to an operation to determine whether a  
5           specified value is stored within the CAM.

1       150. An integrated circuit device comprising:  
2           means for converting an input value into a search value;  
3           a first storage including means for generating a plurality of match signals that indicate  
4           whether the search value matches respective values stored within the first storage;  
5           a second storage including means for outputting a value stored at a location within the  
6           second storage indicated by the plurality of match signals; and  
7           means for comparing the value output from the second storage with the input value.